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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,808	08/28/2003	Klaas Bult	1875.0510002	5778

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EXAMINER	
LAM, TUAN THIEU	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,808	BULT ET AL.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *7-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-6 are under examination. Claims 7-20 have been withdrawn from consideration.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Dingwall (USP 4,521,703) newly cited prior art.

Figure 3 of Dingwall shows a latch circuit comprising a bistable pair of transistors (P1, P2) connected between a reset switch (P3) and a first supply voltage (ground), and having a first port (O1) for receiving a first current signal (current flows along the transistor N1) and producing a first output voltage, and a second port (O2) for receiving a second current signal (current flows along the transistor N2) and producing a second output voltage, and a vertical latch (P11, P21) connected between said first supply voltage and a second supply voltage (Vdd and ground), and connected to said first port (O1), when said transistor P11 is turned on, a current flows from said second supply voltage (Vdd) through said transistor to said first port as called for in claim 1.

Regarding claim 2, said transistor is a MOSFET.

Regarding claim 3, the reset switch P3 is a microelectromechanical reset switch.

Regarding claim 4, the vertical latch is capable of decreasing the time necessary for said first port to reach a steady stage voltage in response to said first current signal received.

3. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Zerbe (USP 5,977,798) newly cited prior art.

Figure 3 of Zerbe shows a latch circuit comprising a bistable pair of transistors (112, 113) connected between a reset switch (114) and a first supply voltage (ground), and having a first port (200) for receiving a first current signal (current flows along the transistor 100) and producing a first output voltage, and a second port (201) for receiving a second current signal (current flows along the transistor 101) and producing a second output voltage, and a vertical latch (110, 111) connected between said first supply voltage and a second supply voltage (Vdd and ground), and connected to said first port (O1), when said transistor 110 is turned on, a current flows from said second supply voltage (Vdd) through said transistor to said first port as called for in claim 1.

Regarding claim 2, said transistor is a MOSFET.

Regarding claim 3, the reset switch 114 is a microelectromechanical reset switch.

Regarding claim 4, the vertical latch is capable of decreasing the time necessary for said first port to reach a steady stage voltage in response to said first current signal received.

Regarding claim 5, figure 3 shows a vertical latch reset switch 104 connected to the vertical latch.

Regarding claim 6, figure 3 shows a second vertical latch (106, 107) connected between said first supply voltage and second supply voltage and said second port.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Jaussi et al. (USP 6,825,696) newly cited prior art.

Figure 1A of Jaussi et al. shows a latch circuit comprising a bistable pair of transistors (178, 180) connected between a reset switch (186) and a first supply voltage (ground), and having a first port (174) for receiving a first current signal (current flows along the transistor 188) and producing a first output voltage, and a second port (176) for receiving a second current signal (current flows along the transistor 190) and producing a second output voltage, and a vertical latch (182, 184) connected between said first supply voltage and a second supply voltage (Vdd and ground), and connected to said first port (O1), when said transistor 182 is turned on, a current flows from said second supply voltage (Vdd) through said transistor to said first port as called for in claim 1.

Regarding claim 2, said transistor is a MOSFET.

Regarding claim 3, the reset switch 186 is a microelectromechanical reset switch.

Regarding claim 4, the vertical latch is capable of decreasing the time necessary for said first port to reach a steady stage voltage in response to said first current signal received.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P. CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan T. Lam
Primary Examiner
Art Unit 2816

4/27/2006